REMARKS

This is in response to the Office Communication mailed on May 30, 2007, requesting compliance with the provisions of 37 CFR §41.202 for claims 125-140, which have been added since this information was previously supplied. This information is below. Additionally, as claims 141-156 have been added in the interim, this information is also provided below for these claims. The present Response should therefore be considered supplemental to that previously provided for claims 63-124.

All of the presently pending claims are either exact or close copies of claims from a number of related patents, with which a Declaration of Interference is again requested. It is noted that the failure of this Declaration, which has long been requested, has led to delay during which additional ones of these patents have issued, resulting in more claims being copied, in turn leading the greater complexity of any resultant Interference proceeding. Consequently, it is respectfully submitted that the large number of currently pending claims, and the effect this will have on an Interference once declared, is due to delays in the granting of this Request for the Declaration of an Interference. It is again requested that an Interference be declared before even more claims are copied. A telephone call to the undersigned is requested if there are any outstanding matters which need to be resolved in order to facilitate the process.

Consequently, in response to the various portions of 37 CFR §41.202(a), the following supplemental information is provided:

(1) Identification of Patent

Claims 125-140 are copied from US patent number 7,006,384 to Banks, granted issued February 18, 2006. Specifically, claims 125-140 are respectively either direct or close copies of claims 1-6, the pair 7 and 8, 9, the pair 10 and 11, 12, the pair 13 and 14, 15, the pair 16 and 17, 18, the pair 19 and 20, and 21 of US patent number 7,006,384.

Claims 141-146, 148, 150, 152, 154, and 156 are copies claims 1-6, 9, 12, 15, 18, and 21, respectively, of U.S. Patent No. 7,068,542 of Banks, granted issued June 27, 2006. Claims 147, 149, 151, 153, and 155 are substantial copies of the pairs of claims 7 and 8, 10 and 11, 13 and 14, 16 and 17, and 19 and 20, respectively, of U.S. Patent No. 7,068,542.

(2) Identification of Claims Believed to Interfere, Proposed Count, and Claim Correspondence

(i) As noted above, claims 125-140 are respectively either direct or close copies of claims 1-6, the pair 7 and 8, 9, the pair 10 and 11, 12, the pair 13 and 14, 15, the pair 16 and 17, 18, the pair 19 and 20, and 21 of US patent number 7,006,384 and the claims are consequently believed to respectively interfere. Claims 141-146, 148, 150, 152, 154, and 156 are copies claims 1-6, 9, 12, 15, 18, and 21, respectively, of U.S. Patent No. 7,068,542, with claims 147, 149, 151, 153, and 155 are substantial copies of the pairs of claims 7 and 8, 10 and 11, 13 and 14, 16 and 17, and 19 and 20, respectively, of U.S. Patent No. 7,068,542 and the claims are consequently believed to respectively interfere.

(ii) Consequently, the present application contains claims that are either exact or substantial copies of claims from two more patents. As these claims and the previously copied claims are from four separate patents, the Patent Office has found that these claims correspond to six different inventions; that is, as these claims form six groups, each from a different patent, the implication is that the Office has found the claims within each group to correspond, but that claims from different groups are distinct. Although the validity of this grouping has not been considered in detail, to facilitate the Interference process, the applicant suggests two additional counts, one corresponding to each group of claims.

Claim 125 of the present application, which is a copy of claim 1 of U.S. Patent No. 7,006,384, is suggested as a Count 5:

Count 5

A non-volatile semiconductor memory device, comprising:

a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;

reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and

sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;

wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,

wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the first read reference value is shifted toward the second program state from a midpoint between the first program state and the second program state,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,

wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and

wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.

Claim 141 of the present application is a copy of claim 1 of U.S. Patent No. 7,068,542 and is suggested as a Count 6:

Count 6

A non-volatile semiconductor memory device, comprising:

a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;

reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and

sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;

wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,

wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the third read reference value is shifted toward the second program state from a midpoint between the third program state and the erase state,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it

has been verified that the electrically alterable parameter has been shifted to the selected one state,

wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and

wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.

(iii) Claims 125-140 are respectively either direct or close copies of claims 1-6, the pair 7 and 8, 9, the pair 10 and 11, 12, the pair 13 and 14, 15, the pair 16 and 17, 18, the pair 19 and 20, and 21 of US patent number 7,006,384 and, consequently, would correspond to Count 5 under the suggested correspondence.

Claims 141-146, 148, 150, 152, 154, and 156 are copies claims 1-6, 9, 12, 15, 18, and 21, respectively, of U.S. Patent No. 7,068,542, with claims 147, 149, 151, 153, and 155 are substantial copies of the pairs of claims 7 and 8, 10 and 11, 13 and 14, 16 and 17, and 19 and 20, respectively, of U.S. Patent No. 7,068,542 and, consequently, would correspond to Count 6 under the suggested correspondence.

(3) Claim Chart for the Counts

Section (3) requires a claim chart for the proposed count comparing at least one claim of each party showing why they interfere within the meaning of Sec. 41.203(a).

As the proposed Count 5 is Claim125 of the present application, they correspond exactly:

Claim 125 of Present Application	Count 5
A non-volatile semiconductor memory device, comprising:	A non-volatile semiconductor memory device, comprising:
a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile	a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile

memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;	memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;
reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and	reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and
sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;	sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;
wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,	wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,
wherein the second read reference value is allocated substantially at a	wherein the second read reference value is allocated substantially at a

midpoint between the second program state and the third program state, and the first read reference value is shifted toward the second program state from a midpoint between the first program state and the second program state,	midpoint between the second program state and the third program state, and the first read reference value is shifted toward the second program state from a midpoint between the first program state and the second program state,
wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,	wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,
wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and	wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and
wherein the reference value generating circuitry generates the first,	wherein the reference value generating circuitry generates the first,

second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.	second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.

As the proposed Count 5 is also claim 1 of U.S. patent number US patent number 7,006,384, they also correspond:

Claim 1 of U.S. patent number 7,006,384	Count 1
A non-volatile semiconductor memory device, comprising:	A non-volatile semiconductor memory device, comprising:
a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;	a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;
reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third	reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third

program states; and	program states; and
sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;	sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;
wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,	wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,
wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the first read reference value is shifted toward the second program state from a midpoint between the first program state and the second program state,	wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the first read reference value is shifted toward the second program state from a midpoint between the first program state and the second program state,
wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter	wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter

indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,	indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,
wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and	wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and
wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.	wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.

As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

As the proposed Count 6 is Claim 141 of the present application, they correspond exactly:

Claim 141 of Present Application	Count 6
A non-volatile semiconductor memory device, comprising:	A non-volatile semiconductor memory device, comprising:
a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;	a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;
reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and	reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and
sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;	sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;
wherein the first read reference value	wherein the first read reference value

is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,	is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,
wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the third read reference value is shifted toward the second program state from a midpoint between the third program state and the erase state,	wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the third read reference value is shifted toward the second program state from a midpoint between the third program state and the erase state,
wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,	wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,
wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and	wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and

third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and	third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and
wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.	wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.

As the proposed Count 6 is Claim 1 of U.S. patent number 7,068,542, they correspond exactly:

Claim 1 of U.S. patent number 7,068,542	Count 6
A non-volatile semiconductor memory device, comprising:	A non-volatile semiconductor memory device, comprising:
a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;	a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;
reference value generating circuitry generating first, second and third	reference value generating circuitry generating first, second and third

programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and	programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and
sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;	sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;
wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,	wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,
wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the third read reference value is shifted toward the second program state from a midpoint between the third program state and the erase state,	wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the third read reference value is shifted toward the second program state from a midpoint between the third program state and the erase state,
wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically	wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically

alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,	alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,
wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and	wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and
wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.	wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.

As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

(4) How Applicant Will prevail on Priority

Section (4) requires an explanation of why the applicant will prevail on priority.

As specified in the "Cross-Reference to Related Application" section added to the beginning of the present application by Preliminary Amendment filed concurrently with the present application, and as is also shown on the filing receipt, the present application is a continuation of U.S. patent application serial number 09/188,417, filed on November 9, 1998, now U.S. patent number 6,304,485, which is which is a continuation of U.S. patent application serial number 08/771,708, filed on December 20, 1996, now U.S. patent number 5,991,517, which is in turn a continuation of U.S. patent application serial number 08/174,768, filed on December 29, 1993, now U.S. patent number 5,602,987, which is in turn a continuation of U.S. patent application serial number 07/963,838, filed on October 20, 1992, now U.S. patent number 5,297,148, which is a division of U.S. patent application serial number 07/337,566, filed on April 13, 1989, now abandoned. Consequently, the present application is entitled to an effective filing date of April 13, 1989.

U.S. patent 7,006,384 of Banks has a filing date of December 23, 2003, and claiming priority from a number of U.S. patent applications (in one case through a continuation in-part), the earliest of which has a filing date of February 27, 1995. Thus, this earliest priority date is several years after the priority date to which the present application is entitled.

Similarly, U.S. patent 7,068,542 of Banks has a filing date of September 20, 2004, and claiming priority from a number of U.S. patent applications (in one case through a continuation in-part), the earliest of which has a filing date of February 27, 1995. Thus, this earliest priority date is several years after the priority date to which the present application is entitled.

(5,6) Claim Charts

The following claim charts show the corresponding written description for each claim in the specification of the present application. They also show where the disclosure provides a constructive reduction to practice within the scope of the interfering subject matter.

Support for Claims

Pending Claims	Present Application
125. A non-volatile semiconductor memory device, comprising:	The exemplary embodiments are non-volatile semiconductor memory devices.
a plurality of non-volatile memory cells each of which has a storage structure	Figures 12 and 22 of the present application and Figures 15a and 15b of '344.

and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and	One embodiment uses the reference cells of Figure 17B of the present application.
sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;	1440 of Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344.
wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the second read reference	Figure 11c and column 26, lines 51-

value is allocated substantially at a midpoint between the second program state and the third program state, and the first read reference value is shifted toward the second program state from a midpoint between the first program state and the second program state,	65, of `344 and Figures 15A and 15B of the present application.
wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,	Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344. A program algorithm is shown in Figure 23 of the present application.
wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the reference value generating circuitry generates the first, second and third programming reference	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.

values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.	`344, column 26, lines 60-65: "shifted by a fixed amount ..."

126. A non-volatile semiconductor memory device according to claim 125, wherein a shift amount of one of the first, second and third read reference values from the corresponding one of the first, second and third programming reference values is dependent upon the corresponding one of the first, second and third programming reference values.	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application. `344, column 26, lines 60-65: "shifted by a fixed amount ..."

Aside from differing in the claim upon which they depend, claim 127 is the same as claim 95. Similarly, claim 128 is the same as claim 96, except for a change of dependence. The Examiner is referred to the appropriate previously supplied claim charts.

129. A non-volatile semiconductor memory device according to claim 125, wherein each read reference value is dependent upon the corresponding programming reference value.	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application. `344, column 26, lines 60-65: "shifted by a fixed amount ..."

Aside from differing in the claim upon which they depend, claims 130, 132, 134, 136, and 138 are the same as claim 98. Similarly, claims 131, 133, 135, 137, and 139 are the same as claim 99, except for a change of dependence. The Examiner is referred to the appropriate previously supplied claim charts.

140. A non-volatile semiconductor memory device according to claim 140, wherein the first, second and third read reference values are dependent upon the first, second and third programming reference values, respectively.	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application. `344, column 26, lines 60-65: "shifted by a fixed amount ..."

Aside from the fifth element after the preamble, claim 141 is the same as claim 125, the difference being "first" changed to "third" in both occurrences and "second program state" (at the end of the element) now being "erased state":

141. A non-volatile semiconductor memory device, comprising:	The exemplary embodiments are non-volatile semiconductor memory devices.
a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;	Figures 12 and 22 of the present application and Figures 15a and 15b of `344. Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading	One embodiment uses the reference cells of Figure 17B of the present application.

the first, second and third program states; and	
sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, second and third read programming reference values;	1440 of Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344.
wherein the first read reference value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the third read reference value is shifted toward the second program state from a midpoint between the third program state and the erase state,	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the	Figure 17B of the present application; Figure 11e, lower left portion, and column 26, lines 51-65, of `344. A program algorithm is shown in Figure 23 of the present application.

electrically alterable parameter has been shifted to the selected one state,	
wherein the first, second and third programming reference values are used for verifying whether the electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.
wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.	Figure 11c and column 26, lines 51-65, of `344 and Figures 15A and 15B of the present application.  `344, column 26, lines 60-65: "shifted by a fixed amount …"

Claims 142-156 are respectively the same as claims 126-140, aside from the change of dependence for claim 125 to claim 141. Consequently, the Examiner is referred to the above, rather than just a repeating of these elements in what is already a long Response.

Conclusion

As presented above, it is respectfully submitted that the present application supports all of the currently pending claims and an early indication of their allowability is earnestly solicited. In the meantime, a phone call to the undersigned is invited should there be any questions.

Respectfully submitted,

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